WHAT IS CLAIMED IS:

1. A multiplier-divider circuit for a PFC controller, comprising:

a first multiplier-input terminal, for accepting a first multiplier signal;

a second multiplier-input terminal, for accepting a second multiplier signal;

a divisor-input terminal, for accepting a divisor-signal;

a constant current source, for providing a constant current;

a pulse generator, for generating a pulse-signal, an inversed pulse-signal, a sawtooth-signal, a sample-signal and a clear-signal;

a first multiplier-divider stage, having a first input, a second input and a third input, wherein said first input is connected to said first multiplier-input terminal, said second input is connected to said constant current source, and said third input connected to said divisor-input terminal;

a second multiplier-divider stage, having a first input, a second input and a third input, wherein said first input is connected to an output of said first multiplier-divider stage, said second input is connected to said second multiplier-input terminal, and said third input connected to said divisor-input terminal; and

an output terminal, connected to an output of said second multiplier-divider stage.

2. The multiplier-divider circuit according to claim **1**, wherein the magnitude of an output signal of the first multiplier-divider stage is substantially proportional to the product of the magnitude of said first multiplier-signal and the magnitude of said constant current.

3. The multiplier-divider circuit according to claim **1**, wherein the magnitude of said output signal of said first multiplier-divider stage is inversely proportional to the

magnitude of the divisor-signal.

4. The multiplier-divider circuit according to claim **1**, wherein the magnitude of an output signal of said second multiplier-divider stage is substantially proportional to the product of the magnitude of said first multiplier-signal, the magnitude of said second multiplier signal, and the magnitude of said constant current.

5. The multiplier-divider circuit according to claim **1**, wherein the magnitude of said output signal of the second multiplier-divider stage is inversely proportional to the square of the magnitude of said divisor-signal.

6. The multiplier-divider circuit according to claim **1**, wherein said pulse generator comprises:

a pulse-signal output terminal;

a sawtooth-signal generator;

an inversed pulse-signal output terminal;

a sample-signal output terminal;

a clear-signal output terminal;

a pulse-generator current source, having an input connected to a voltage source;

a pulse-generator current sink, having an output connected to a ground reference;

a pulse generator junction;

a first pulse generator switch, connected between an output of the pulse generator current source and said pulse generator junction;

a second pulse generator switch, connected between said pulse generator junction and an input of said pulse generator current sink; and

a control circuit, for the pulse generator switches.

7. The multiplier-divider circuit according to claim **6**, wherein said control circuit for the pulse generator switches comprises:

a hysteresis comparator, having an input connected to said pulse generator junction;

a pulse-generator capacitor, connected between said input of said hysteresis comparator and the ground reference;

a first array of two NOT-gates, having an input connected to an output of said hysteresis comparator;

a pulse-generator comparator, having a positive input connected to an output of the sawtooth-signal generator, said pulse generator comparator having a negative input supplied with a reference voltage;

a second array of two NOT-gates, having an input connected to an output of said pulse-generator comparator;

a latch circuit, consisting of a first NAND-gate and a second NAND-gate, said latch circuit having a first input connected to an output of said first array of two NOT-gates, said latch circuit having a second input connected to an output of said second array of two NOT-gates, said latch circuit having an output for supplying a control signal to said second pulse-generator switch; and

a first pulse-generator NOT-gate, for supplying a control signal to the first pulse-generator switch, said first pulse-generator NOT-gate having an input connected to said output of said latch circuit.

8. The multiplier-divider circuit according to claim **7**, wherein the control circuit for the pulse generator switches further comprises:

a first array of three NOT-gates, having an input connected to said output of the latch circuit;

a first pulse-generator AND-gate, having an input, an inverted input, an output, wherein said input is connected to an output of said first array of three NOT-gates, said inverted input is connected to said output of the latch circuit, and said output is connected to said sample-signal output terminal;

a second array of three NOT-gates, having an input connected to said first input of said latch circuit;

a second pulse-generator AND-gate, having an input, an inverted input and an output, wherein said input is connected to an output of said second array of three NOT-gates, said inverted input is connected to said first input of the latch circuit, and said output is connected to said clear-signal output terminal of the pulse generator.

a third NAND-gate, having a first input, a second input and an output, wherein said first input is connected to said output of said latch circuit, said second input is connected to said first input of said latch circuit, and said output is connected said pulse-signal output terminal; and

a second pulse-generator NOT-gate, for supplying an inversed pulse-signal, said second pulse generator NOT-gate having an input connected to said output of the third NAND-gate.

9. The multiplier-divider circuit according to claim **6**, wherein the sawtooth-signal generator comprises:

a sawtooth-signal output terminal, for outputting a sawtooth-signal;

a sawtooth capacitor, connected between said sawtooth-signal output terminal and the ground reference;

a sawtooth current sink, for discharging said sawtooth capacitor, said sawtooth current sink having an output connected to the ground reference;

a sawtooth discharge switch, connected between said sawtooth-signal output terminal and an input of said sawtooth current sink, said sawtooth discharge switch having a control terminal supplied with said inversed pulse-signal; and

a sawtooth charging switch, connected between said divisor-input terminal and said sawtooth-signal output terminal, said sawtooth charging switch having a control terminal supplied with said pulse-signal.

10. The multiplier-divider circuit according to claim **9**, wherein the sawtooth current sink comprises:

a sawtooth transistor, for producing a variable discharge current, said sawtooth transistor having a drain connected to said sawtooth-signal output terminal via said sawtooth discharge switch;

a sawtooth operation amplifier, for driving said sawtooth transistor, said sawtooth operation amplifier having a negative input connected to a source of said sawtooth transistor, and a positive input connected to the divisor-input terminal; and

a sawtooth resistor, connected between said source of said sawtooth transistor and the ground reference.

11. The multiplier-divider circuit according to claim **9**, wherein the length of a charge time and the length of a discharge time of said sawtooth capacitor are independent of the magnitude of the divisor input signal.

12. The multiplier-divider circuit according to claim **9**, wherein the peak value of the sawtooth-signal is proportional to the the magnitude of said divisor-input signal.

13. The multiplier-divider circuit according to claim **1**, wherein said first

multiplier-divider stage comprises:

a first charge-time control circuit, for generating a first charge-time signal;

a first linear charging block, for generating a first charging signal; and

a first sample-and-hold circuit, for producing an first output signal.

14. The multiplier-divider circuit according to claim **13**, wherein said first charge-time control circuit of said first multiplier-divider stage comprises:

a first charge-time comparator, for supplying a first initial signal, said first charge-time comparator having a positive input connected to said first multiplier-input terminal, and a negative input supplied with said sawtooth-signal; and

a first AND-gate, for generating said first charge-time signal, said first AND-gate having a first input supplied with said inverse pulse-signal, and a second input connected to an output of said charge-time comparator.

15. The multiplier-divider circuit according to claim **13**, wherein said first linear charging block of the first multiplier-divider stage comprises:

a first charge-output terminal, for supplying said first charging signal;

a first charge capacitor, for generating said first charging signal, said first charge capacitor connected between said output terminal and the ground reference;

a first charge switch, for controlling the charge-time of said charge capacitor, said charge switch connected between said constant current source and said first charge-output terminal, wherein said first charge switch comprises an control terminal controlled by said first charge-time control circuit; and

a first discharge switch, for discharging said first charge capacitor, said discharge switch connected between said first charge-output terminal and the ground reference, said discharge switch having a control terminal controlled by said

clear-signal, wherein the state of said first multiplier-divider stage is reset in response to said clear-signal.

16. The multiplier-divider circuit according to claim **13**, wherein said first sample-and-hold circuit of said first multiplier-divider stage comprises:

a first sample-and-hold operation amplifier, for buffering said first charging signal, said first sample-and-hold operation amplifier having a positive input supplied with said first charging signal, and a negative input connected to an output of first said sample-and-hold operation amplifier;

a first sample-and-hold switch, for sampling said first charging signal, said first sample-and-hold switch being connected between an output of said first sample-and-hold operation amplifier and said output of said first multiplier-divider stage; and

a first sample-and-hold capacitor, for holding said output signal of said first multiplier-divider stage, said first sample-and-hold capacitor being connected between the output terminal of said first multiplier-divider stage and the ground reference.

17. The multiplier-divider circuit according to claim **1**, wherein said second multiplier-divider stage comprises:

a second charge-time control circuit, for generating a second charge-time signal;

a second linear charging block, for generating a second charging signal; and

a second sample-and-hold circuit, for producing an second output signal.

18. The multiplier-divider circuit according to claim **17**, wherein said second charge-time control circuit of said second multiplier-divider stage comprises:

a second charge-time comparator, for supplying a second initial signal, said

second charge-time comparator having a positive input connected to said output terminal of said first multiplier-divider stage, and a negative input supplied with said sawtooth-signal; and

a second AND-gate, for generating said second charge-time signal, said second AND-gate having a second input supplied with said inverse pulse-signal, and a second input connected to an output of said charge-time comparator.

19. The multiplier-divider circuit according to claim **17**, wherein said second linear charging block of the second multiplier-divider stage comprises:

a second charge-output terminal, for supplying said second charging signal;

a second charge capacitor, for generating said second charging signal, said second charge capacitor being connected between said output terminal and the ground reference;

a second charge switch, for controlling the charge-time of said charge capacitor, said charge switch being connected between said second multiplier-input terminal and said second charge-output terminal, said second charge switch having an control terminal controlled by said second charge-time control circuit; and

a second discharge switch, for discharging said second charge capacitor, said discharge switch being connected between said second charge-output terminal and the ground reference, said discharge switch having a control terminal controlled by said clear-signal, wherein the state of said second multiplier-divider stage is reset in response to said clear-signal.

20. The multiplier-divider circuit according to claim **17**, wherein said second sample-and-hold circuit of said second multiplier-divider stage comprises:

a second sample-and-hold operation amplifier, for buffering said second

charging signal, said second sample-and-hold operation amplifier having a positive input supplied with said second charging signal and a negative input connected to an output of second said sample-and-hold operation amplifier;

a second sample-and-hold switch, for sampling said second charging signal, said second sample-and-hold switch being connected between an output of said second sample-and-hold operation amplifier and said output of said second multiplier-divider stage; and

a second sample-and-hold capacitor, for holding said output signal of said multiplier-divider, said second sample-and-hold capacitor being connected between the output terminal of said second multiplier-divider stage and the ground reference.

21. The multiplier-divider circuit according to claim **1**, wherein the length of said first charge-time of said first multiplier-divider stage is proportional to the magnitude of said first multiplier-signal divided by the magnitude of the divisor-signal;

22. The multiplier-divider circuit according to claim **1**, wherein the length of said second charge-time of said second multiplier-divider stage is proportional to the magnitude of said second multiplier-signal divided by the magnitude of said divisor-signal;

23. The multiplier-divider circuit according to claim **1**, wherein said sample-signal is generated in response to said pulse-signal, following a delay time, wherein said clear-signal is generated in response to said sample-signal following a delay time.

24. The multiplier-divider circuit according to claim **1**, wherein said multiplier-divider circuit is built from CMOS MOSFET-based devices.